CLAIMS:

1. An information processing apparatus, comprising:

a display;

a storage for storing a floorplan regarding allocation of blocks constituting a semiconductor integrated circuit, and evaluation indices for evaluating modification of the floorplan;

an input device for inputting specifications for modifying the floorplan;

a processing device for modifying the floorplan according to the specifications to generate a plurality of floorplans, and for selecting one of the floorplans according to the evaluation indices.

2. An information processing apparatus in accordance with Claim 1, wherein circuit information in which the blocks are described in a high-level language is stored in the storage.

3. An information processing apparatus in accordance with Claim 1, wherein the evaluation indices include know-how of a designer who designs the semiconductor integrated circuit.

4. An information processing apparatus including an input device, a display, a storage and a processing device, and for designing a semiconductor integrated circuit, wherein

the processing device stores a function of each of blocks constituting the semiconductor integrated

circuit, a floorplan which is allocation information of the blocks, and evaluation indices used when the floorplan is modified, in the storage with being associated with each other, the function, the floorplan and the evaluation indices being inputted from the input device.

5. An information processing apparatus in accordance with Claim 4, wherein the evaluation indices include know-how of a designer who designs the semiconductor integrated circuit.

6. An information processing system, comprising:

a circuit designing apparatus for designing a semiconductor integrated circuit, for receiving circuit information of blocks constituting the semiconductor integrated circuit, a floorplan which is allocation information of the blocks, and evaluation indices for evaluating modification of the floorplan, and for storing the circuit information, the floorplan and the evaluation indices with being associated with each other; and

a floorplan modifying apparatus for receiving the circuit information, the floorplan and the evaluation indices from the circuit designing apparatus, for receiving information for modifying the floorplan from an input device, for modifying the floorplan according to the received information, and for evaluating the modified floorplan according to the evaluation indices.

7. An information processing system in accordance with Claim 6, wherein the evaluation indices include know-how of a designer who designs the semiconductor integrated circuit.

8. A storage media on which a function of each of blocks constituting a semiconductor integrated circuit, a floorplan which is allocation information of the blocks, and evaluation indices used when the floorplan is modified are stored with being associated with each other.

9. An information storage media in accordance with Claim 8, wherein the evaluation indices include know-how of a designer who designs a semiconductor integrated circuit.

10. A storage media on which

a function of each of blocks constituting a semiconductor integrated circuit, a floorplan which is allocation information of the block, and evaluation indices used when the floorplan is modified are stored with being associated with each other; and

a program for modifying the floorplan according to specifications for modifying the floorplan to generate a plurality of floorplans, and for selecting one of the floorplans according to the evaluation indices is further stored.

11. An information storage media in accordance with Claim 10, wherein the evaluation indices include know-how of a designer who designs a semiconductor

integrated circuit.

12. A floorplan modification method, comprising the steps of:

modifying a floorplan which is beforehand generated according to information for modifying a floorplan regarding allocation of blocks constituting a semiconductor integrated circuit;

evaluating the modified floorplan according to evaluation indices; and

determining a floorplan according to an evaluation value.

13. A large scale integrated circuit produced according to a modified floorplan, wherein

the modified plan is obtained by modifying a floorplan which is predetermined according to information for modifying a floorplan regarding allocation of blocks constituting a semiconductor integrated circuit, according to predetermined evaluation indices.